# Sub-Millimeter GaN-on-Si Dielet Fabrication in Advanced Packaging Substrates Using Femtosecond Laser for 3D Heterogeneous Integration Applications


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***Abstract*—With the maturation of III-V semiconductors, such as gallium nitride (GaN), strong use cases for the 3D heterogeneous integration (3DHI) of these technologies with Si CMOS and interposers are emerging in the fields of wireless, power, quantum and photonic applications. This work proposes a fabrication technology that enables the formation of "tiny", single-transistor GaN dielets. For the first time, a method to fabricate sub-mm$^2$ dielets using femtosecond laser dicing is presented. Several of the key challenges associated with such scaled dielets are discussed with key insights presented on post foundry processing, backside via alignment, and optimization of femtosecond laser parameters. Dielets are formed using GlobalFoundries 130GaNRF technology with dielet sizes as small as 195 µm x 400 µm x 140 µm. Integration of the dielets in glass interposer and 3D stacking with Si CMOS is also presented in this work.**



***Keywords—Gallium nitride, dielet, 3D heterogeneous integration, femtosecond laser.***


## I. Introduction

Gallium nitride (GaN) high electron mobility transistors (HEMT) have shown great potential for high frequency and high power circuits [1]. The high electron mobility and wide bandgap of GaN allows for devices with high cutoff and oscillation frequencies, while providing breakdown voltages and efficiencies in excess of those in silicon. Unfortunately, GaN MMIC fabrication is expensive and mostly limited to low volume due to the use of GaN-on-SiC. Recently, GaN-on-Si has proven to provide comparable performance at high volume [2]. But still, GaN processes have limited back-end-of-line (BEOL) and do not offer a reliable CMOS technology. CMOS is required for baseband, backend and phased array circuits, which are critical for modern communications and sensing. To revolutionize GaN circuits, integration of GaN into heterogeneous platforms is critical. This will allow for the rapid adoption of GaN at a high volume, in addition to providing added functionality to conventional chips.

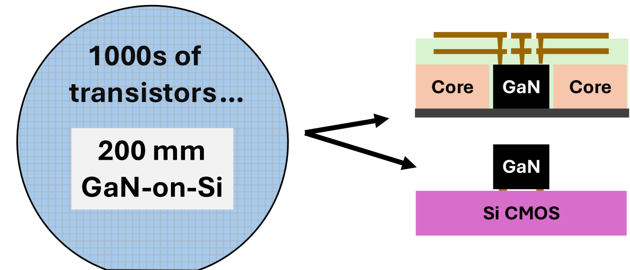


Fig. 1 Fabrication of the GaN FEOL on 200 mm wafers and the integration of dielets in advanced packaging platforms for circuit build up.

Previous heterogeneous integration schemes of GaN have focused on chiplet/wafer scale integration, both of which include BEOL in GaN [3]. In a power amplifier chip, the majority of the area is consumed by the BEOL. Using these previous approaches, the number of transistors that can be fabricated on a wafer is severely limited and results in added costs of fabricating BEOL on GaN. The optimal solution is to fabricate only the front-end-of-line (FEOL) on GaN, leaving the BEOL for the heterogeneous platform [4], [5]. For this to be economical, the entire wafer must be used for the fabrication of GaN transistors that are then singulated and integrated with the BEOL which can be fabricated in Si CMOS or glass interposer [6]. It is quite difficult to mechanically isolate a single GaN transistor, or dielet, from a GaN-on-Si wafer. A single GaN transistor is on the order of < 500 µm in the x and y dimensions.

Conventional blade dicing can singulate dies of size several millimeters by several millimeters. Stealth dicing can achieve die sizes of 1 mm x 1 mm. Achieving die sizes of sub 1 mm x 1 mm has only been possible by plasma dicing. But this requires the use of thick resist masks, additional sample preparation, and deep reactive ion etching (DRIE) after fabrication of the GaN wafer.

A solution to this issue is through the use of a femtosecond laser. Femtosecond lasers offer an extremely short pulse duration resulting in minimal laser recast material and little to no microcracks. The thermal load is also reduced on the sample, as the femtosecond pulse is shorter than the typical 7-8 picoseconds of electron-lattice thermalization time of materials such as silicon and glass [7]. These tools have long been used for nanoscale micromachining, including cavities, resonators and via formation. This work presents the first demonstration of fabrication of single transistor dielets using the proposed femtosecond dicing method and their integration into advanced packaging substrates. Using GlobalFoundries 130GaN(-on-Si) HEMT technology, sourced from 200 mm wafers, copper interconnects are formed for 3DHI. Femtosecond laser is utilized for the debris-free, dielet singulation of dimensions 375 µm x 400 µm x 140 µm, 275 µm x 400 µm x 140 µm, 220 µm x 400 µm x 140 µm, and 195 µm x 400 µm x 140 µm. This work will present a novel backside dicing methodology for dielets using top side via drilling for TSV-based alignment marks, and backside ablation for singulation. The influence of laser power, repetitions, step size and spot size will be discussed. Proof-of-concept integration into interposers such as glass with redistribution layers (RDL) and with Si CMOS are demonstrated. This work sets the stage for dielet-based heterogeneous integration for wireless / digital / AI / power / quantum / photonic applications.

## II. Foundry Post-Processing

GlobalFoundries 130GaNRF transistors are utilized for this work. The technology is a high volume GaN-on-Si technology that features $L_g$ = 160 nm with a copper back-end-of-line (BEOL). Once the chips are received from foundry, the process shown in Fig. 2 is followed to fabricate 3DHI-ready dielets. The process is comprised of interconnect formation, topside alignment via drilling and backside dielet dicing.

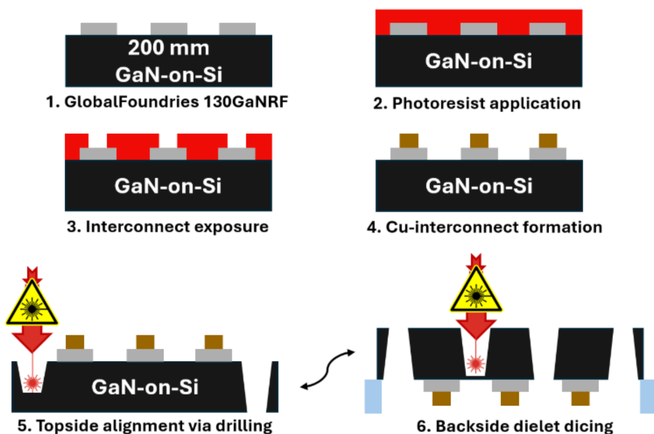


Fig. 2 Process flow for GaN dielet fabrication.

The GF130GaNRF pad layer is comprised of aluminum. To ease the technology's compatibility with 3DHI, copper interconnects are fabricated. A standard liftoff process is utilized to fabricate the interconnects. AZNLOF 2035 photoresist is patterned using an MLA150 maskless aligner. Electron beam deposition is used to deposit Ti/Cu (100 nm/1000 nm). The completed copper interconnects can be seen in Fig. 3.

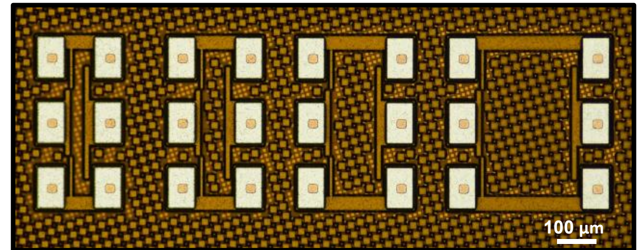


Fig. 3 GlobalFoundries 130GaNRF transistors with copper interconnects.

To fabricate the dielets, an Optec femtosecond laser with a wavelength of 1035 nm is utilized. Femtosecond laser induces minimal damage to the target substrate while being able to induce damage strong enough to remove the target material. Yet still, laser recast is still expelled as a by-product of the process. The debris formed is quite difficult to remove. Sonication cannot be used as the RF GaN transistors feature fragile T-gates that can be damaged from the vibrations. Another solution to remove the laser recast, is to first apply resist before the femtosecond dicing is performed and then strip the resist after dicing. But, during the laser ablation process, Fig. 4 (a), the resist becomes molten with the laser recast forming a solid coating of debris, shown in Fig. 4 (b), which is unable to be

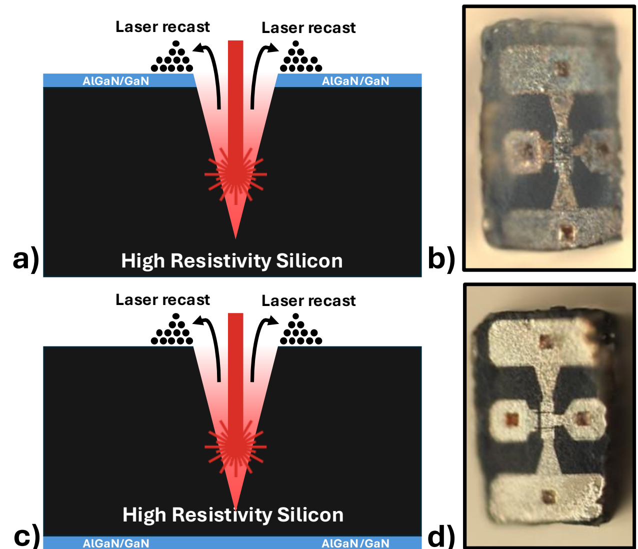


Fig. 4 Femtosecond laser dicing approaches. (a) Front side laser dicing scheme. (b) Dielet fabricated using front side dicing approach with significant laser debris on front side of sample. (c) Backside laser dicing scheme. (d) Dielet fabricated using backside dicing approach with minimal laser debris on front side of sample.

removed through conventional resist strip techniques including solvent and plasma based. The solution to this is to use a resist-free dicing process, and to complete the dicing from the backside of the samples, Fig. 4 (c), to result in the majority of the laser recast being deposited on the backside of the sample as opposed to the front. The result is the fabrication of a debris free dielet, Fig. 4 (d).

## III. Femtosecond Laser Optimization

For the laser dicing cut pattern, 11 rectangular cut lines are used with 5 µm spacing between the lines extending from the initial cutline which 55 µm greater than the desired transistor size in both the x and the y. Additionally, 15 movements are made in the z direction with a step size of 10 µm to account for the sample thickness of 140 µm.

To determine the optimal laser parameters, several power levels and repetitions are attempted. A laser pulse of 1500 fs is utilized. Laser powers ranging from 10-70% of the maximum tool power of 4 W, with 1 and 2 repetitions are used. As the power utilized increases, the amount of laser debris generated increases as well. The laser recast is present on both the dielets as well as the native substrate from which the dielets are cut. Efforts should be taken to minimize the debris in order to ensure surface planarity when completing tasks such as embedding or 3D stacking. The etch depth and debris profile was analyzed using laser profilometry in Fig. 5. A laser power of 70% (2.8 W) and 1 repetition was able to singulate the dielet. A repetition of 2 was also attempted in an effort to reduce the laser power required. This technique proved to not be a viable solution as even with 10% laser power, upwards of 90 µm is already deposited on the dielet and at 20% laser power, almost 150 µm in laser recast in seen on the dielet, shown in Fig. 6.

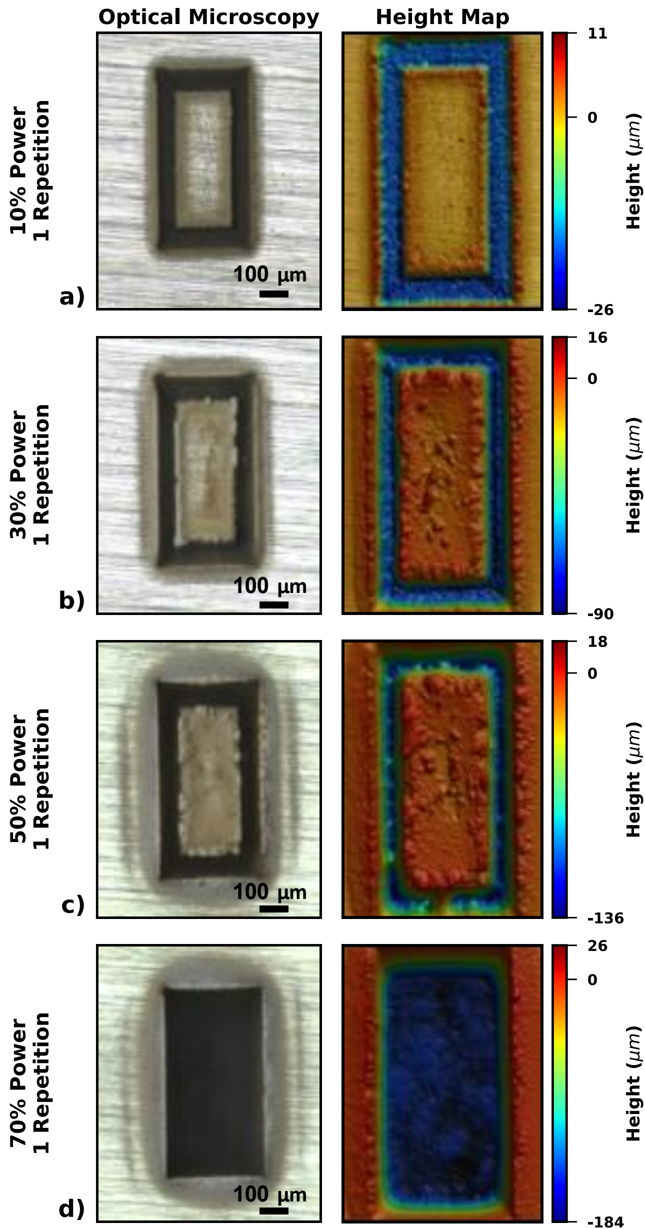


Fig. 5 Femtosecond laser dicing optimization for various power levels using 1 cutting repetitions. (a) Optical microscope and height map with 10% power. (b) Optical microscope and height map with 30% power. (c) Optical microscope and height map with 50% power. (d) Optical microscope and height map with 70% power.

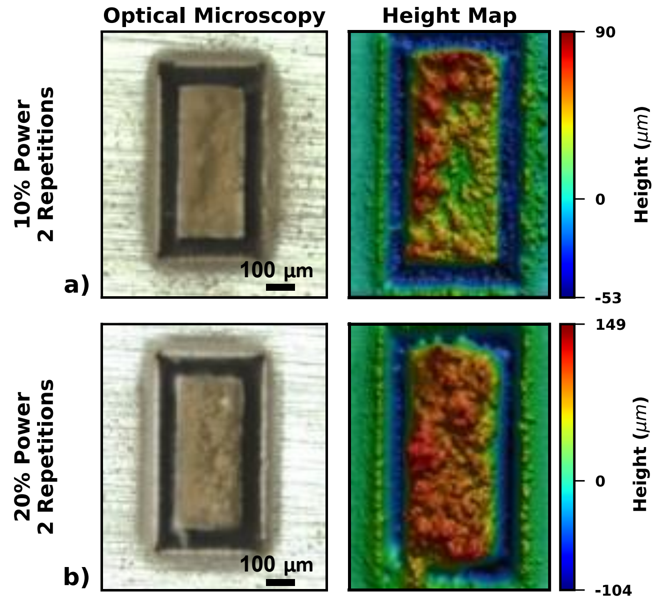


Fig. 6 Femtosecond laser dicing optimization for various power levels using 2 cutting repetitions. (a) Optical microscope and height map with 10% power. (b) Optical microscope and height map with 20% power.

Further analysis of the laser profile is shown in Fig. 7. For 10% laser power, a depth of 17.9 µm is achieved with a cavity angle of 50-70°. There is 9-12.3 µm of laser recast material. Increasing to 30%, a depth of 41 µm is achieved with a cavity angle of 71-76°. 17.3-22.7 µm of laser recast material is measured. At 50%, a depth of 95.5 µm is achieved with a cavity angle of 76-81°. The laser recast is around 21.5-33.6 µm. At 70%, the entirety of the 140 µm cavity is cleared with a taper of 82-84°. The amount of laser recast is a maximum of 19 µm. This is significantly reduced as compared to the case with 2 repetitions.

Using these optimized conditions, the final dielets are singulated, shown in Fig. 8. Since the dielets are cut from the back side of the sample, no topography is present to complete laser alignment. As such, the femtosecond laser is used to drill through silicon vias from the topside. These vias are used for backside alignment and the subsequent dicing of the dielets. The fabricated dielets are of dimension, 195 µm x 400 µm x 140 µm, 220 µm x 400 µm x 140 µm, 275 µm x 400 µm x 140 µm and 375 µm x 400 µm x 140 µm. The fabricated dielets have sidewall roughness on the order of several microns which should be addressed in future work. Once singulated, the dielets are handled using a Finetech pick and place tool.

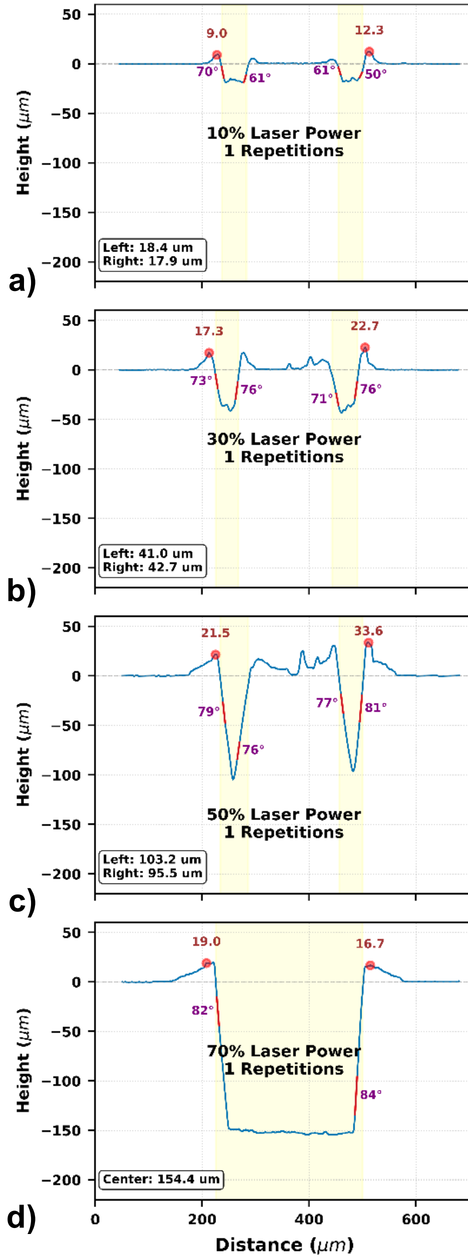


Fig. 7 Laser cutting profiles with 1 repetition. (a) Profile with 10% laser power. (b) Profile with 30% laser power. (c) Profile with 50% laser power. (d) Profile with 70% laser power.

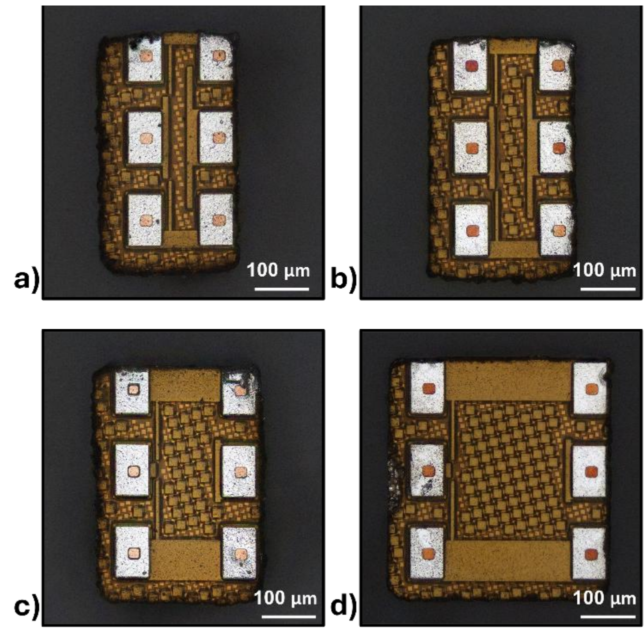


Fig. 8 Fabricated GaN-on-Si dielets. (a) Dielet of size 195 µm x 400 µm x 140 µm. (b) Dielet of size 220 µm x 400 µm x 140 µm. (c) Dielet of size 275 µm x 400 µm x 140 µm. (d). Dielet of size 375 µm x 400 µm x 140 µm.

## IV. INTEGRATION INTO ADVANCED PACKAGES

To serve as an example of how dielets can be integrated for circuit build up, the fabricated dielets are integrated into various advanced packages, Fig. 9. The first package features the GaN dielet being embedded into a ACG glass interposer. The interposer features a 2 redistribution layers (RDL) fabricated using ajinomoto build up film (ABF) and a copper BEOL. The second platform for integration is a 3D-mmWIC integration scheme, where the dielet is bonded to a high resistivity silicon interposer. The interposer features Ni/Au (30 nm /300 nm) traces fabricated using a standard liftoff process and also includes Ti/Cu (100 nm/1000 nm) pillars for 3DHI. The bonding is completed in a formic acid environment under low force and CMOS-compatible temperatures ( < 2N, <400°C).

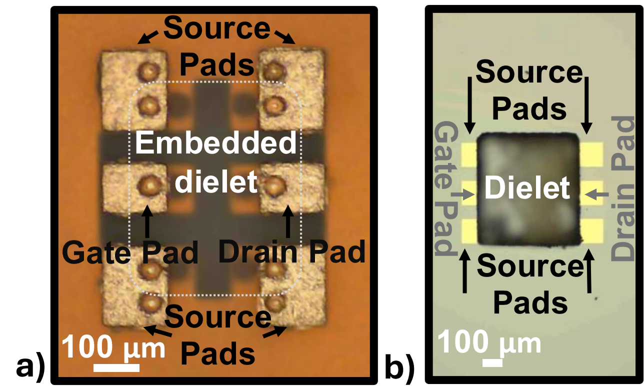


Fig. 9 Top view of integration of dielets into advanced packages. (a) Embedded dielet in glass interposer. (b). 3D-mmWIC with dielet and silicon interposer.

## V. Conclusion

This paper presents a novel method to fabricate sub-$mm^2$ dielets using femtosecond laser ablation. This technology allows for far smaller dielets as compared to conventional dicing technologies such as blade and even laser stealth dicing. GlobalFoundries 130GaNRF HEMTs are used to demonstrate the dielet process. A post foundry copper interconnect process, topside via drilling for backside alignment, and femtosecond dicing scheme is demonstrated. Efforts taken to minimize laser recast and the optimal laser conditions are presented. Dielets of size 195 µm x 400 µm x 140 µm, 220 µm x 400 µm x 140 µm, 275 µm x 400 µm x 140 µm and 375 µm x 400 µm x 140 µm. Integration of the dielets is shown into a 2 RDL glass interposer and a 3D-mmWIC featuring a high resistivity silicon interposer.


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