A 4 W Heterogeneous Power Amplifier with GaN-on-Si Dielets in Single-Crystal Diamond Interposer for 6G FR3 Applications

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***Abstract*— This paper presents the design and fabrication of a heterogeneous power amplifier (PA) incorporating gallium nitride (GaN) high electron mobility transistor (HEMT) dielets into a single-crystal diamond interposer platform. 12×100 µm GlobalFoundries 130RF GaN high electron mobility transistors (HEMT) are singulated using femtosecond laser to a size of 274 µm × 400 µm for the fabrication of single transistor dielets. The diamond interposer is able to provide heat spreading, packaging and circuit build up for the dielet. The interposer features 2 redistribution layers (RDL) for metallization fabrication. The effects of the interposer on dielet load pull performance are analyzed. At 10 GHz, a 1.8 dB increase in output power (P_{out}), 1.5% increase in maximum power added efficiency (PAE), and a 0.3 dB increase in gain is observed. These insights guide the design of a power amplifier (PA) for 6G FR3 applications with a 3 dB bandwidth (BW) of 6.8-10.3 GHz that is able to provide up to 4 W of output power. From 8-10 GHz, the PA has a PAE ranging from 39.2-49.1% with respectable performance at 6 dB back off.**

***Keywords*— FR3, GaN dielets, interposer, power amplifier, 6G, single-crystal diamond.**

I. Introduction

The heterogeneous integration (HI) chip design ecosystem is expanding with the ability to incorporate high performance semiconductors, such as GaN, an ideal solution for high power and high frequency, with Si CMOS, the semiconductor workhorse that provides digital and control circuitry [1]. Integration of single transistor, GaN front end of line (FEOL) dielets is extremely attractive as it allows for the fabrication of the back end of line (BEOL) of the heterogeneous system on a better suited substrate such as Si CMOS or an interposer [2], [3]. One important area that must be addressed in HI is effective thermal management. With the integration of many GaN dielets, several localized hot spots can exist that lead to degradation in chip reliability. The ideal heterogeneous platform should include the ability to effectively spread the heat generated by GaN dielets to equalize the overall chip temperature. Single crystal diamond offers the highest thermal conductivity among all materials, with a theoretical thermal conductivity as high as 2400 W/m·K [4]. While diamond has traditionally been a costly, and low volume option, significant improvements in growth conditions have made 100 mm wafers possible at scale [5].

Significant progress has also been made towards direct diamond growth on GaN HEMTs [6]. Top side diamond deposition offers an effective device-level solution for decreasing device junction temperature, but requires high growth temperatures that are not Si CMOS compatible and degrades device performance due to added parasitics. Further extension of the technology to high volume applications has yet to be demonstrated as well. As such, the ability to develop a scalable circuit design process integrating diamond and GaN, without negatively affecting GaN device performance, has yet to exist. A single-crystal diamond interposer can allow for the development of a high volume platform for heterogeneous circuit design and in-situ heat spreading through the device back side. Through the fabrication of RDL layers on diamond, GaN dielets can be packaged and circuits can be fabricated with improved heat spreading for PAs.

This paper will describe such an integration of GlobalFoundries 130RF GaN dielets into a single-crystal diamond interposer and the effects of integration on large signal performance as well as the subsequent design and fabrication of a heterogeneous PA for 8-10 GHz 6G FR3 operation. This work demonstrates the ability to singulate commercial GaN dielets and fabricate a single dielet amplifier as shown in the technology roadmap in Fig. 1(a) and (b). Fig. 1(c) and (d) envision the expansion of the diamond interposer technology to the build up of circuits that incorporate both III-Vs and Si CMOS as well as the fabrication of 3D-PAs. This paper lays the groundwork for the development for high performance heterogeneous PAs with enhanced performance, as compared to the state of the art chips today, through the use of a localized heat spreading diamond interposer.

II. GaN Dielet Characterization

For this work, a GlobalFoundries 130RF GaN-on-Si HEMT dielet with gate length, L_g = 200 nm, gate to drain distance of L_{gd} = 1.88 µm, and gate width, W_g, of 12×100 µm was utilized. The dielet was singulated using a femtosecond laser with 3.5 W power into a size of roughly 274 µm × 400 µm. In addition, the dielets were thinned to 200 µm and copper pads were deposited on the source, drain and gate contacts for ease of HI. To ensure sound hardware/model correlation, characterization of the dielet performance was completed

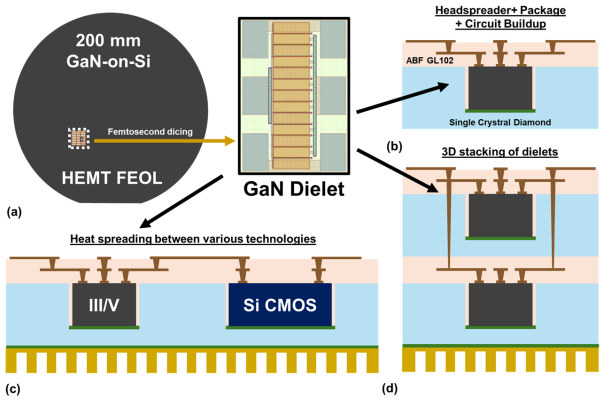

Fig. 1. Heterogeneous GaN in single crystal diamond interposer roadmap. (a) Dielet fabrication using femtosecond laser. (b) Power amplifier buildup in diamond interposer. (c) Heterogeneous integration of III-V's and Si CMOS in diamond interposer. (d) Heat spreading solution for 3D PAs.

before and after integration into the diamond interposer. Large signal load pull measurements provide significant design insights for GaN PA design. Fig. 2 displays the load pull of the dielets before and after integration. At 10 GHz, with a V_{DS}=20 V and I_D=30 mA, a slight shift in the optimal load impedance for a balanced power and PAE match is observed in Fig. 2(a). Fig. 2(b) shows that after integration into the diamond interposer, the large signal gain improves from 11.4 dB to 11.7 dB, the maximum PAE improves from 48.9% to 50.4% and the saturated output power increases from 34.6 dBm to 36.4 dBm. The load pull curve is also noticeably smoother with fewer instabilities, a further sign of the improved heat spreading capabilities of the diamond interposer.

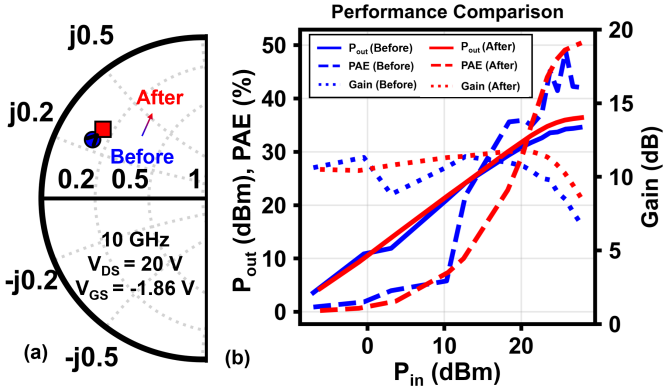

Fig. 2. 10 GHz load pull measurements of GaN HEMT before and after integration into diamond interposer. (a) Shift in optimal load impedance before and after integration into diamond interposer. (b) P_{out}, PAE, and Gain curves before and after integration into diamond interposer.

III. Diamond Interposer Fabrication

The fabrication flow of the diamond interposer can be seen in Fig. 3. The process utilizes a single-crystal diamond substrate featuring a blind cavity for the integration of the dielet. The dielet is bonded to the diamond interposer using a pick-and-place tool using a bonding schedule of 2 N of force at 150 °C for 30 minutes. A high thermal conductivity die attach film (DAF) is used as the thermal interface between the dielet and the diamond substrate, ensuring effective heat transfer from the dielet to the diamond. For the build up of metal layers, a semi-additive patterning process is utilized. A 2 layer RDL is fabricated using 15 µm Ajinomoto build up film (ABF) GL102 and 4 µm copper metallization.

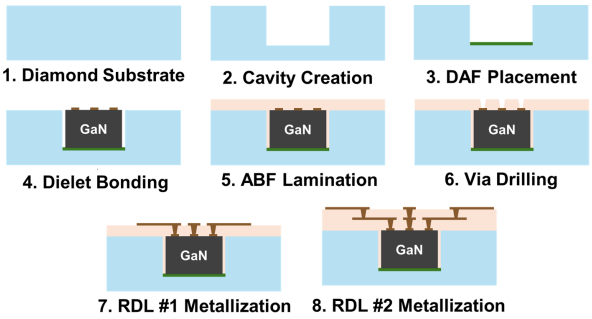

Fig. 3. Fabrication process of diamond interposer.

IV. Amplifier Design and Fabrication

The amplifier design involves the use of microstrip matching networks. A T-type topology is chosen for both input and output matching networks to allow for a pair of transmission zeros located at the lower and upper sidebands for improved out-of-band rejection. The dielet S-parameter as well as 10 GHz load pull measurements are used to tune the values of the microstrip lines, providing impedance matching targets for frequencies in the band of interest, 8-10 GHz. Keysight Advanced Design System (ADS) and Ansys HFSS (High Frequency Structure Simulator) were used for the device, circuit and package co-design. The simulated matching networks display good agreement with the design targets as shown in Fig. 4. The designed circuit has a targeted center frequency close to 9 GHz with a target of 10 dB of gain in the desired 6G FR3 band of interest. The circuit topology as well as the designed impedance and electrical lengths of each line can be seen in Fig. 5. Fig. 6 displays the final fabricated chip with an overall size of 5.2 mm × 4.1 mm.

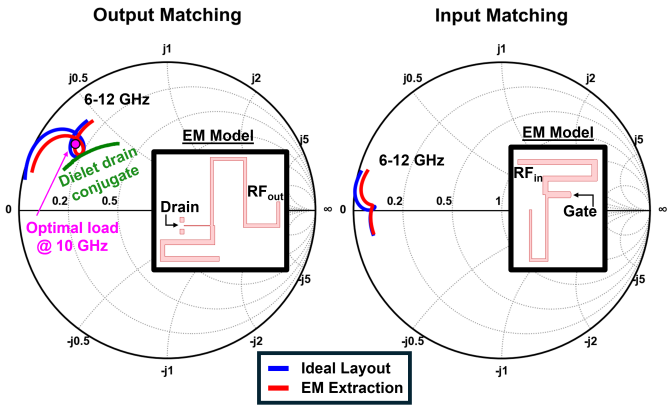

Fig. 4. Output and input matching network ideal layout versus EM extracted layout performance as well as design targets.

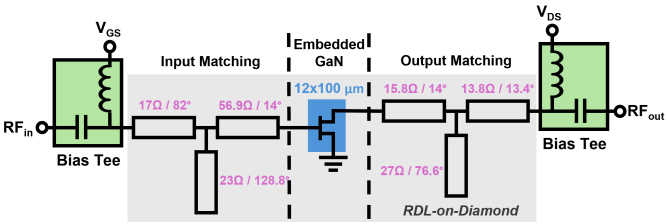

Fig. 5. Circuit topology.

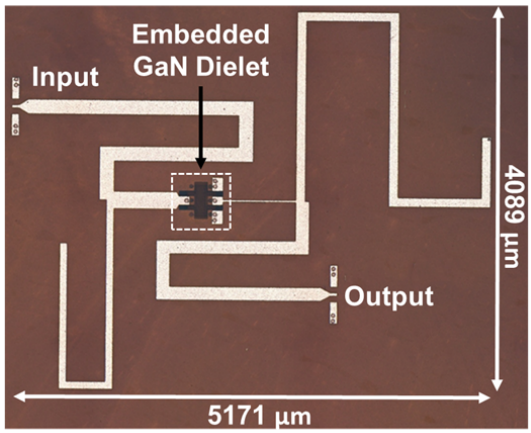

Fig. 6. Fabricated heterogeneous power amplifier with embedded GaN-on-Si dielet in single crystal diamond interposer.

V. Amplifier Characterization

The heterogeneous PA is characterized under small and large signal conditions. The S-parameters of the amplifier at V_{DS}=20 V and I_D=30 mA bias are shown in Fig. 7. A peak gain of 9.8 dB is observed at 9.1 GHz. A gain flatness of 1 dB is maintained from 8-10 GHz. The 3 dB bandwidth of the amplifier is from 6.8-10.3 GHz. A good match is seen between the simulated and measured values. The amplifier is unconditionally stable in the operating band with K and µ factor > 1 in Fig. 8.

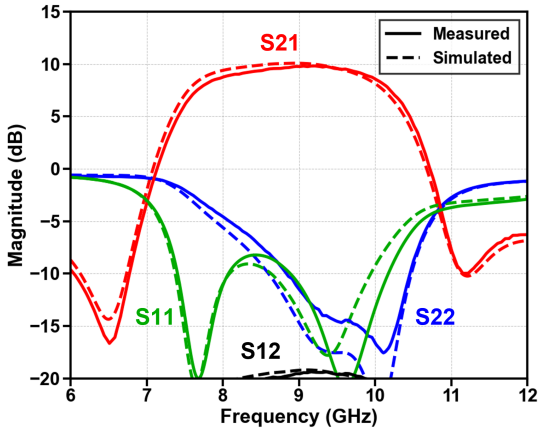

Fig. 7. S-parameters of fabricated amplifier.

The amplifier was tested under large signal CW conditions. At 9 GHz, a peak PAE of 49.1% is achieved with a saturated

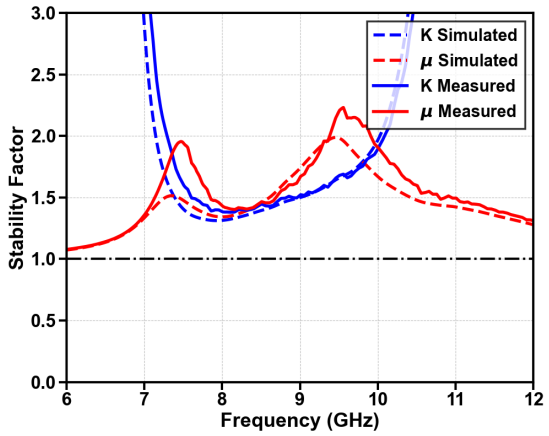

Fig. 8. Stability factors of fabricated amplifier.

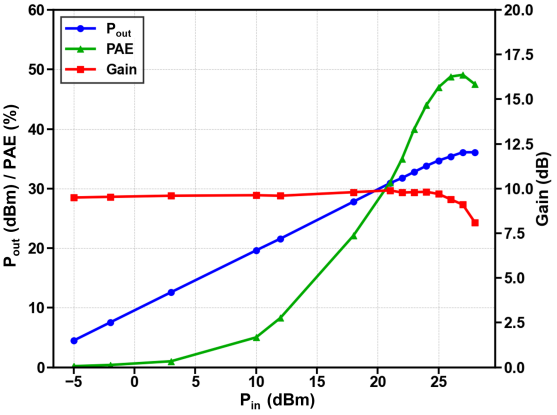

Fig. 9. Large signal power sweep at 9 GHz.

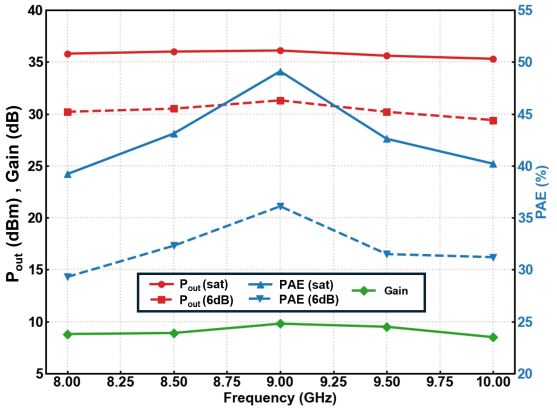

Fig. 10. Large signal CW measurements across frequency.

power of 36.1 dBm in Fig. 9. Fig. 10 shows the large signal performance of the amplifier with P_{in}=27 dBm from 8-10 GHz. Saturated output power levels in excess of 35 dBm are exhibited with PAE ranging from 39.2-49.1%. The amplifier is also tested under 6 dB back off conditions for estimation of performance under high peak-to-average-power ratio (PAPR) modulated signals. The amplifier displays backed off power levels between 29.4-31.3 dBm. PAE values range between

Table 1. Overview of prior published embedded RF GaN heterogeneously integrated PAs.

	This work	[7]	[8]	[9]	[10]
Core Substr.	**Single-Crystal Diamond**	AGC Glass	HR Silicon	HR Silicon	Silicon Carbide
Metal Layers	**2 layer RDL**	2 layer RDL	4 layer Si Interp.	4 layer Si Interp.	2 layer SiC Interp.
Emb. Chip Type	**Single Trans. Dielet**	Single Trans. Dielet	Multi- Trans. Chiplet	Single Trans. Chiplet	Single Trans. Dielet
HEMT Tech.	**GaN-on-Si**	GaN-on-Si	GaN-on-SiC	GaN-on-SiC	GaN-on-SiC
Gate Width (mm)	**1.2**	0.05	0.2	0.075	0.6
V_D (V)	**20**	10	20	8	N.A.
3dB BW (GHz)	**6.8-10.3**	9.3-10.2	26-31	26**	77**
Gain (dB)	**9.8**	5.48	6.5	8	6.5
P_{out} (dBm)	**35.3-36.1**	23.3	25	19.8	N.A.
PAE (%)	**39.2-49.1**	33.5	N.A.	23.5	N.A.
P_{out} 6dB (dBm)	**29.4-31.3**	15.1*	N.A.	N.A.	N.A.
PAE 6dB (%)	**29.3-36.1**	5.7*	N.A.	N.A.	N.A.
Dielet Size (mm^2)	**0.27×0.40**	0.35×0.54	0.29×0.56	0.24×0.24	0.16×0.17
Chip Size (mm^2)	**4.1×5.2**	4.5×4.3	1.36×0.73	1.44×0.55	0.16×0.17
* Values reported at 7dB back off ** Center frequency					

29.3-36.1%. The fabricated amplifier has been benchmarked against other notable heterogeneously integrated GaN PA solutions in Table 1. To the best of the authors' knowledge, the amplifier achieves the highest gain, P_{out} and PAE of any heterogeneously integrated GaN amplifier to date.

VI. Conclusion

In this paper, the first demonstration of a GaN-on-Si dielet in single-crystal diamond interposer amplifier has been reported. GlobalFoundries GaN-on-Si dielets 12×100 µm were utilized for the fabrication of the amplifier. Significant improvements in the load pull characteristics are seen through improved gain, PAE and P_{out} in addition to improved thermal management, seen in smoother power sweep curves. These insights help drive the design for the 6.8-10.3 GHz PA. The PA is able to achieve 4 W of output power with PAE as high as 49.1%. Respectable performance at 6 dB back off is also achieved. These are the highest reported metrics for a GaN dielet-based heterogeneously integrated solution to date. Future work will focus on advanced circuit topologies and efforts to minimize the overall chip area.

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